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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,666	09/18/2003	Douglas R. Hackler SR.	51889/5	4619

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EXAMINER

THOMAS, ERIC W

ART UNIT PAPER NUMBER

2831

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/664,666

Applicant(s)

HACKLER ET AL.

Examiner

Eric W. Thomas

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-7 and 9-54 is/are pending in the application.
- 4a) Of the above claim(s) 13-25 and 39-54 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-12 and 26-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 9/18/03 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Art Unit: 2831

## INTRODUCTION

The examiner acknowledges, as recommended in the MPEP, the applicant's submission of the amendment dated 3/22/05. At this point, claims 1, & 26 have been amended; and claims 13-25, 39-54 are withdrawn. Thus claims 1-7, 9-12, and 26-38 are pending in the instant application.

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/22/05 has been entered.

### ***Claim Rejections - 35 USC § 102***

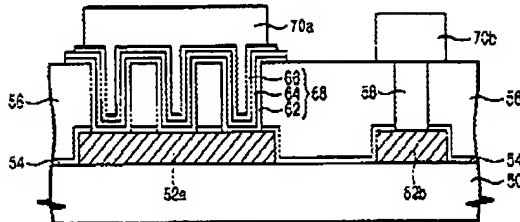
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Jin et al. (US 2003/0183862).

Fig. 4F



Jin et al. disclose in fig. 4f, a substrate (50), a conductive material (52a) formed above the substrate; an insulating material (54, 56) formed on the conductive material wherein the insulating material and the conductive material serve as a form for defining a plurality of capacitor trenches above the conductive layer, the insulating material defines the trench sidewalls and the conductive material defines the trench bases, a bottom electrode (62) formed onto the capacitor trenches so as to form a layer within the capacitor trenches in contact with the conductive material, wherein the bottom electrode extends up the sides of the capacitor trenches to form bottom electrode sidewalls; a capacitor dielectric (64) at least partially positioned on the bottom electrode; and a top electrode (66, 70a) at least partially positioned on the capacitor dielectric, substantially filling the capacitor trenches and forming an interconnect.

Regarding claim 2, Jin et al. disclose the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material (see paragraphs 40, 41 & 48).

Regarding claim 3, Jin et al. disclose the capacitor dielectric has a high-k dielectric constant (paragraph 48).

Regarding claim 4, Jin et al. disclose the capacitor dielectric has a dielectric constant greater than or equal to about 6.0 (see paragraph 48 – materials).

Regarding claim 6, Jin et al. disclose the capacitor structure is a discrete capacitor.

Regarding claim 7, Jin et al. disclose the capacitor structure is configured to be part of an integrated circuit (paragraph 1-4).

Regarding claim 9, Jin et al. disclose the conductive material layer is comprised of a different material than the bottom electrode (paragraphs 39 & 47).

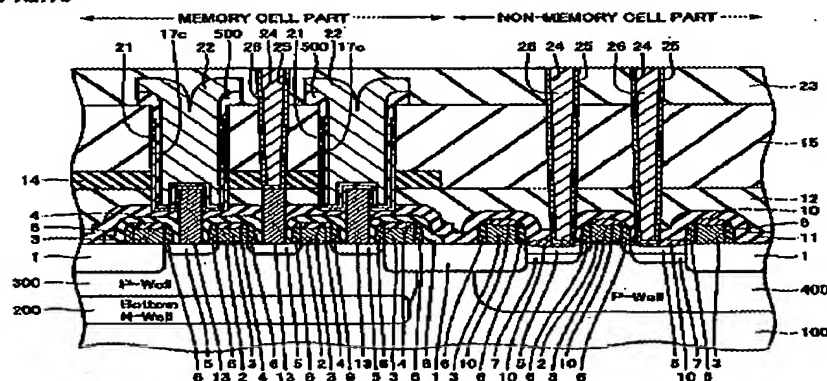
Regarding claim 10, Jin et al. disclose the top electrode is disposed in the capacitor trenches such that the top electrode interdigitates with the bottom electrode.

Regarding claim 11, Jin et al. disclose the bottom electrode further comprises a bottom electrode top wall (see fig. 4F).

Regarding claim 12, Jin et al. disclose the bottom electrode further comprises a bottom electrode base (see fig. 4F).

3. Claims 26-29, 31-33, 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Kubo (US 6,774,423).

FIG.19



Kubo discloses in fig. 19, a capacitor structure comprising: a substrate (100), an insulating material (12, 14, 15) formed on the substrate, wherein the insulating material serves as a form for defining a capacitor trench; a bottom electrode (21), wherein the bottom electrode comprises a bottom electrode layer in the capacitor trench and a bottom electrode plug (13) disposed in the capacitor trench, wherein the bottom electrode layer extends up the sides of the capacitor trench to form bottom electrode sidewalls; a capacitor dielectric (500) at least partially position on the bottom electrode and at least partially formed on the bottom electrode plug; a top electrode (22) at least partially position on the capacitor dielectric and at least partially formed around the bottom electrode plug.

Regarding claim 27, Kubo discloses the capacitor dielectric is made from a material having a higher dielectric constant than the dielectric constant of the insulating material (col. 3 lines 20-35, and col. 8 lines 5-10).

Regarding claim 28, Kubo discloses capacitor dielectric has a high-k dielectric constant (col. 8 lines 5-10 --  $\text{Ta}_2\text{O}_5$   $k \sim 26$ ).

Regarding claim 29, Kubo discloses the capacitor dielectric has a dielectric constant greater than or equal to about 6.0 (col. 8 lines 5-10 --  $\text{Ta}_2\text{O}_5$   $k \sim 26$ ).

Regarding claim 31, Kubo discloses the capacitor structure is a discrete capacitor.

Regarding claim 32, Kubo discloses the capacitor structure is configured to be part of an integrated circuit.

Regarding claim 33, Kubo discloses a conductive material layer (5), wherein the conductive layer is in contact with the bottom electrode.

Regarding claim 35, Kubo discloses the bottom electrode and the capacitor dielectric are formed in the shape of a box (abstract and fig. 19).

Regarding claim 36, Kubo discloses the top electrode is at least partially disposed in the capacitor trench such that the top electrode interdigitates the bottom electrode (see fig 19).

Regarding claim 37, Kubo discloses the bottom electrode further comprises a bottom electrode top wall (see fig. 19).

Regarding claim 38, Kubo discloses the bottom electrode further comprises a bottom electrode base (see fig. 19).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

Art Unit: 2831

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. (US 2003/0183862) in view of Alers et al. (US 6,320,244).

Jin et al. disclose the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Jin et al., since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (US 6,774,423) in view of Alers et al. (US 6,320,244).

Kubo discloses the claimed invention except for the capacitor dielectric is formed from a stack comprising more than one material.

Alers et al. teach that it is known in the capacitor art to form a dielectric layer from a stack of dielectric materials having more than one material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the dielectric of Alers et al. in the capacitor of Kubo, since such a modification would provide a high quality dielectric having a high dielectric constant and low leakage.



Art Unit: 2831

8. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (US 6,774,423) in view of Crenshaw et al. (US 6,184,074).

Kubo discloses the bottom electrode is formed from a silicon material (col. 7 lines 55-65). Kubo discloses the claimed invention except for the conductive material is formed from a different material than the bottom electrode.

Crenshaw et al. teach the use of a conductive material that is formed from a different material than a bottom electrode (col. 2, lines 59-60 and element 26).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the conductive material of Crenshaw et al. in the capacitor of Kubo, wherein the conductive material is different than the electrode, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

### ***Response to Arguments***

9. Applicant's arguments filed 3/22/05 have been fully considered but they are not persuasive.

A) Regarding the argument, "the top electrode and interconnection are not separate elements. The top electrode 160 serves as the top electrode 160 and as an interconnect. Paragraphs [0037], [0057], and [0063]. By this paper, claim 1 has been amended to recite that the top electrode forms an interconnect. An additional fabrication step for an upper interconnect is not required. An additional fabrication step to form an insulation layer to prevent bridge phenomenon is also

not required. The claimed feature is not taught or suggested in Jin and represents a significant improvement in capacitor structure” is not persuasive.

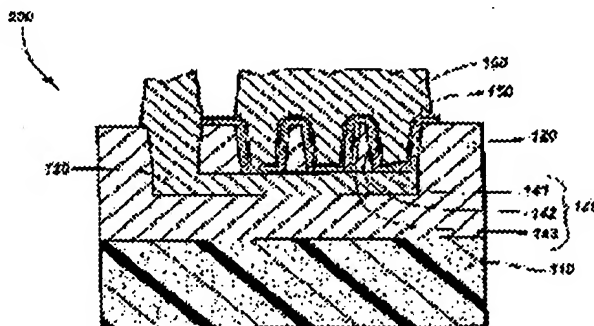
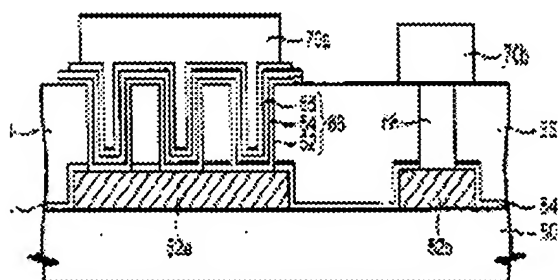
1) Jin discloses the claimed structure. Applicant is reminded that the method of forming the device is not germane to the issue of patentability of the device itself. In re STEPHENS, WENZL, AND BROWNE, 145 USPQ 656 (CCPA 1965).

2) As recognized by ones of ordinary skill in the art, the interconnect and top electrode of Jin forms a top electrode structure. Larson (US 5,005,102) discloses (fig. 1) a top electrode structure that is formed from a plurality of conductive layers, wherein the top electrode layer forms a top electrical interconnect that connects the capacitor to other components of an integrated circuit.

B) Regarding the argument, “Claim 1 is further amended to recite that the top electrode substantially fills the capacitor trenches. Support is found for this amendment in paragraph (0037) and the accompanying figures. In Jin, all disclosed embodiments illustrate that the upper electrodes only partially fill the capacitor trenches. An interconnection conductive layer is required to completely fill the capacitor trenches. In the present invention, the conformance of the top electrode layer 160 to the trench sidewalls is not at issue as the top electrode layer 160 simply fills the trench after the dielectric 150 is deposited. Paragraph [0037]. The present invention simplifies fabrication, as a single step is required to complete a trench filling.

2) Jin discloses the top electrode (66, 70a) “substantially fills” the trench (see below & element of 160 of present invention).

Fig. 4K



**Fig. 6**

3) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the trenches are "completely filled") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

C) Regarding the argument, "Independent claim 26 stands rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat No. 6,777,423 to Kubo ("Kubo"). Claim 26 recites a bottom electrode that comprises a bottom electrode layer and a bottom

Art Unit: 2831

electrode plug. The Office Action relies on the polycrystalline silicon plug 13 for the teaching of a bottom electrode plug. In Kubo the plug 13 is always stated to be a polycrystalline silicon plug. Silicon is not an electrode. An electrode is defined as "a conductor through which an electric current enters or leaves a nonmetallic portion of a circuit, as a dielectric, an electrolyte, or a semiconductor." Webster's College Dictionary, 1992. It is well known that silicon is not a conductor, but may be used as a semiconductor. A semiconductor is not conductor or an electrode. The differences between the silicon plug of Kubo and the present invention are further evident by their placement and function. In Kubo, the silicon plug 13 is covered with the lower electrode 21. The silicon plug 13 does not directly contact the dielectric film 500. The silicon plug 13 is not a metal and does not function as lower electrode. In the present invention, the bottom electrode plug 144 extends from the lower electrode and directly contacts and is covered by the capacitor dielectric 150. The bottom electrode plug 144 is part of the bottom electrode 140 and functions as an electrode. As Kubo does not teach or suggest an electrode plug extending into a capacitor trench, Kubo cannot anticipate claim 26" is not persuasive.

1) The plug and bottom electrode layer (as combined) form a "bottom electrode layer", wherein the bottom electrode plug is disposed within the capacitor trench, and a dielectric at least partially formed on the bottom electrode. The plug extends into the capacitor trench as seen in fig. 19.

2) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., the electrode plug directly contact the dielectric film; and the plug is a metal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

3) US patents 5,130,267; 5,519,238; 6,365,954; 5,258,321; 5,177,576; 5,250,458; 5,227,322; and 5,213,992 teach electrodes formed from polycrystalline silicon material.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W. Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on Monday - Friday 5:30 AM - 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2831

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ewt

 3/29/05  
ERIC W. THOMAS  
PRIMARY EXAMINER